

**FULL VERSION OF PENDING CLAIMS:**

1        Claims 1 - 28 (cancelled)

1        Claim 29 (previously added): A processor for executing an instruction sequence  
2        generated by converting a program that is capable of being described by mutually exclusive first  
3        and second conditional instructions, so that the instruction sequence includes only the first  
4        conditional instruction out of the first and second conditional instructions,  
5                wherein the processor has only the first conditional instruction out of the first and  
6        second conditional instructions.

1        Claim 30 (previously added): The processor of Claim 29,  
2                wherein the first conditional instruction is a conditional transfer instruction.

1        Claim 31 (previously added): The processor of Claim 29,  
2                wherein the first conditional instruction is a conditional arithmetic instruction.

1        Claim 32 (previously added): A processor for executing an instruction sequence  
2        generated by converting a program that is capable of being described by mutually exclusive first  
3        and second conditional instructions, so that the instruction sequence includes only the first  
4        conditional instruction out of the first and second conditional instructions,  
5                wherein the processor is operable to decode only the first conditional instruction  
6        out of the first and second conditional instructions.

1        Claim 33 (currently amended): The processor of Claim 32,  
2                wherein the first conditional instruction is a conditional transfer instruction.

1           Claim 34 (currently amended): The processor of Claim 32,

2                       wherein the first conditional instruction is a conditional arithmetic instruction.

1           Claim 35 (previously added): A processor for executing an instruction sequence

2   generated by converting a program that is capable of being described by mutually exclusive first

3   and second conditional instructions, so that the instruction sequence includes only the first

4   conditional instruction out of the first and second conditional instructions,

5                       wherein the processor is operable to execute only the first conditional instruction

6   out of the first and second conditional instructions.

1           Claim 36 (currently amended): The processor of Claim 35,

2                       wherein the first conditional instruction is a conditional transfer instruction.

1           Claim 37 (currently amended): The processor of Claim 35,

2                       wherein the first conditional instruction is a conditional arithmetic instruction.

1           Claim 38 (currently amended): A processor that executes an instruction sequence,

2   comprising:

3                       a decoding unit operable to decode an instruction sequence generated by

4   converting a program that is capable of being described by mutually exclusive first and second

5   conditionally instructions, so that the instruction sequence includes only the first conditional

6   instruction out of the first and second conditional instructions; and

7                       an executing unit operable to execute the instruction sequence decoded by the

8   decoding unit;

9                wherein the decoding unit is operable to decode only the first conditional  
10 instruction out of the first and second conditional instructions.

1            Claim 39 (currently amended): An instruction conversion apparatus for converting a  
2 program that is capable of being described by mutually exclusive first and second conditional  
3 instructions into an instruction sequence executable by a processor,

4            wherein the instruction conversion apparatus, when only the first conditional  
5 instruction out of the first and second conditional instructions is decodable by the processor,  
6 interchanges (a) a condition of the second conditional instruction with a condition of the first  
7 conditional instruction, and (b) an instruction executed when the condition of the second  
8 conditional instruction is satisfied with an instruction executed when the condition of the second  
9 conditional instruction is ~~satisfied with an instruction executed when the condition of the second~~  
10 ~~conditional instruction~~ is not satisfied.

1            Claim 40 (currently amended): An instruction conversion apparatus, comprising:  
2            an intermediate code generating unit operable to generate an intermediate code  
3 sequence by converting a program that is capable of being described by mutually exclusive first  
4 and second conditional instructions;  
5            a detecting unit operable to detect, from the intermediate code sequence, (a) a  
6 conditional instruction that judges whether to execute one of a first operation and a second  
7 operation, (b) a first operation code that executes an instruction when the judgment result of the  
8 conditional instruction is to execute the first operation, and (c) a second operation code that  
9 executes an instruction when the judgment result of the conditional instruction is to execute the  
10 second operation; and

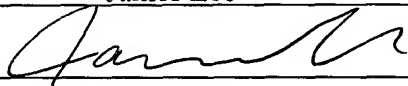
11                    an interchanging unit operable, when only the first conditional instruction out of  
12   the first and second conditional instruction is decodable by a processor, to interchange (a) the  
13   second conditional instruction with the first conditional instruction, and (b) an operation of the  
14   first operation with an operation of the second operation.

**REMARKS**

Claims 33-34, and 36-40 are amended to correct typographical errors. Applicant respectfully requests this amendment be entered prior to examination on the merits.

If the Examiner believes that a telephone interview will help further the prosecution of this case, the Examiner is respectfully requested to contact the undersigned attorney at the listed telephone number.

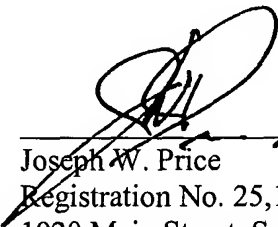
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By: James Lee  
  
Signature

Date of Signature: August 6, 2003

Very truly yours,

**SNELL & WILMER L.L.P.**

  
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